CLAIMS

What is claimed is:

1. A method for a high-K gate dielectric stack for a MOSFET device gate structure to reduce Voltage threshold (V_{th}) shift in a completed MOSFET device comprising the steps of:

providing a high-K gate dielectric layer over a semiconductor substrate substrate;

forming a buffer dielectric layer on the high-K gate dielectric comprising a dopant selected from the group consisting of a metal, a semiconductor, and nitrogen;

forming a gate electrode layer on the buffer dielectric layer; and,

lithographically patterning the gate electrode layer and etching to form a gate structure.

2. The method of claim 1, wherein the wherein the buffer dielectric layer dopant type and dopant level is selected to reduce a Voltage threshold (V_{th}) shift.

3. The method of claim 1, wherein buffer dielectric layer dopant type and dopant level is selected to reduce a Voltage threshold (V_{th}) shift to less than about half of the forbidden energy bandgap (Eg).

4. The method of claim 1, further comprising forming an interfacial layer on the semiconductor substrate prior to the step of forming a high-K dielectric layer.

5. The method of claim 4, wherein the interfacial layer is selected from the group consisting of silicon dioxide, nitrided silicon dioxide, silicon nitride and silicon oxynitride.

6. The method of claim 1, wherein the buffer dielectric layer has a dielectric constant of greater than about 3.9.

7. The method of claim 1, wherein the buffer dielectric layer comprises a non-metal containing dielectric selected from the group consisting of semiconductor-oxide, semiconductor-nitride, oxides, nitrides, and silicates.

8. The method of claim 1, wherein the buffer dielectric layer comprises a nitrogen doped dielectric selected from the group consisting of silicon nitrides, silicon oxynitrides, silicate nitrides, and silicate oxynitrides.

9. The method of claim 1, wherein the dopant concentration is graded in decreasing concentration from the high-K dielectric layer/buffer layer interface toward the gate electrode layer.

10. The method of claim 1, wherein the buffer dielectric layer comprises a dielectric including metal dopants.

11. The method of claim 10, wherein the dielectric is selected from the group consisting of oxides, nitrides, oxynitrides, silicon oxides, silicon nitrides, silicon oxynitrides, silicate nitrides, silicate oxides, and silicate oxynitrides.

12. The method of claim 10, wherein the metal dopant concentration is from about 5 atomic percent to about 40 atomic percent.

13. The method of claim 10, wherein the metal dopants are selected from the group consisting of Hf, Al, Ti, Ta, Zr, La, Ce, Bi, W, Y, Ba, Sr, and Pb.

14. The method of claim 10, wherein the metal dopants are selected from the group consisting of Hf and Al.

15. The method of claim 10, wherein different metal dopants comprise PMOS and NMOS gate structures.

16. The method of claim 15, wherein Hf comprises the metal dopants in a NMOS gate structure and Al comprises the metal dopants used in a PMOS gate structure.

17. The method of claim 1, wherein the buffer dielectric layer comprises HfO_2 in a NMOS gate structure and Al_2O_3 in a PMOS gate structure.

18. The method of claim 1, wherein the high-k dielectric layer is selected from the group consisting of metal oxides, metal silicates, metal nitrides, transition metal-oxides, transition metal silicates, metal aluminates, transition metal nitrides, and combinations thereof.

19. The method of claim 1, wherein the high-k dielectric layer is selected from the group consisting of hafnium oxide, aluminum oxide, titanium oxide, tantalum oxide, zirconium oxide, lanthanum oxide, cerium oxide, bismuth silicate, tungsten oxide, yttrium oxide, lanthanum aluminate, barium strontium titanate, strontium titanate, lead zirconate, PST, PZN, PZT, PMN, and combinations thereof.

20. The method of claim 1, wherein the gate electrode layer comprises materials selected from the group consisting of polysilicon, polysilicon-germanium, metals, metal silicides, and combinations thereof.

21. The method of claim 1, wherein the semiconductor substrate comprises material selected from the group consisting of silicon on insulator (SOI), SiGe on insulator (SiGeOI), and germanium on insulator (GeOI), and combinations thereof.

22. A gate structure with a reduced Voltage threshold (V_{th}) shift comprising:

a high-K gate dielectric layer disposed over a semiconductor substrate; and,

a buffer dielectric layer on the high-K gate dielectric the buffer layer comprising dopants selected from the group consisting of a metal, a semiconductor, and nitrogen; and,

a gate electrode layer on the buffer dielectric layer.

23. The gate structure of claim 21, wherein the wherein the buffer dielectric layer dopant type and dopant level reduces a Voltage threshold (V_{th}) shift compared to the absence of the doped dielectric buffer layer.

24. The gate structure of claim 21, wherein buffer dielectric layer dopant type and dopant level reduces Voltage threshold (V_{th}) shift less than about half of the forbidden energy bandgap.

25. The gate structure of claim 21, further comprising an interfacial layer on the semiconductor substrate.

26. The gate structure of claim 21, wherein the interfacial layer is selected from the group consisting of silicon dioxide, nitrided silicon dioxide, silicon nitride and silicon oxynitride.

27. The gate structure of claim 21, wherein the buffer dielectric layer has a dielectric constant of greater than about 3.9.

28. The gate structure of claim 21, wherein the buffer dielectric layer comprises a non-metal containing dielectric selected from the group consisting of semiconductor-oxide, semiconductor-nitride, oxides, nitrides, and silicates.

29. The gate structure of claim 21, wherein the buffer dielectric layer comprises a nitrogen doped dielectric selected from the group consisting of silicon nitrides, silicon oxynitrides, silicate nitrides, and silicate oxynitrides.

30. The gate structure of claim 21, wherein the dopant concentration is graded in decreasing concentration from the high-K dielectric layer/buffer layer interface toward the gate electrode layer.

31. The gate structure of claim 21, wherein the buffer dielectric layer comprises a dielectric including metal dopants.

32. The gate structure of claim 31, wherein the dielectric is selected from the group consisting of oxides, nitrides, oxynitrides, silicon oxides, silicon nitrides, silicon oxynitrides, silicate nitrides, silicate oxides, and silicate oxynitrides.

33. The gate structure of claim 31, wherein the metal dopant concentration is from about 5 atomic percent to about 40 atomic percent.

34. The gate structure of claim 31, wherein the metal dopants are selected from the group consisting of Hf, Al, Ti, Ta, Zr, La, Ce, Bi, W, Y, Ba, Sr, and Pb.

35. The gate structure of claim 31, wherein the metal dopants are selected from the group consisting of Hf and Al.

36. The gate structure of claim 21, wherein different metal dopants comprise PMOS and NMOS gate structures.

37. The gate structure of claim 36, wherein Hf comprises the metal dopants in a NMOS gate structure and Al comprises the metal dopants in a PMOS gate structure.

38. The gate structure of claim 21, wherein the buffer dielectric layer comprises HfO_2 in a NMOS gate structure and Al_2O_3 in a PMOS gate structure.

39. The gate structure of claim 21, wherein the high-k dielectric layer is selected from the group consisting of metal oxides, metal silicates, metal nitrides, transition metal-oxides, transition metal silicates, metal aluminates, transition metal nitrides, and combinations thereof.

40. The gate structure of claim 21, wherein the high-k dielectric layer is selected from the group consisting of hafnium oxide, aluminum oxide, titanium oxide, tantalum oxide, zirconium oxide, lanthanum oxide, cerium oxide, bismuth silicate, tungsten oxide, yttrium oxide, lanthanum aluminate, barium strontium titanate, strontium titanate, lead zirconate, PST, PZN, PZT, PMN, and combinations thereof.